**CLAIMS**

What is claimed is:

Sub A1

1. An apparatus for outputting a clock signal for video reconstruction in a terminal, comprising:

an oscillator that generates the clock signal;

a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock; and

a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range.

2. The apparatus of claim 1, wherein the frequency range bounder includes an output multiplexer and a threshold register that stores at least one threshold value and that is coupled to the output multiplexer, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range.

3. The apparatus of claim 2, wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value.

4. The apparatus of claim 3, wherein the frequency range bounder includes an output multiplexer that selects one of the upper value, the control signal, and the lower

value as the bounded control signal and outputs the bounded control signal to the oscillator to bound the oscillator frequency between an upper level and a lower level.

5. The apparatus of claim 4, wherein the frequency range bounder includes at least one of a high comparator and a low comparator coupled to the output multiplexer, wherein the high comparator compares the control signal with a high limit and the low comparator compares the control signal with a low limit, and wherein the output multiplexer outputs the upper value as the bounded control signal if the control signal is above the high limit and outputs the lower value as the bounded control signal if the control signal is below the low limit.

A' contd

6. The apparatus of claim 3, wherein the frequency range bounder includes at least one of a minimum function block coupled to the high limit register and a maximum function block coupled to the low limit register, wherein the minimum function block outputs the smaller of the control signal and the upper value and wherein the maximum function block outputs the larger of the control signal and the lower value as the bounded control signal.

7. The apparatus of claim 3, wherein the frequency range bounder includes a comparator coupled to the high limit register and low limit register, wherein the comparator compares the control signal with the upper and lower values and outputs the control signal to the output register if the control signal is between the upper and lower values.

8. The apparatus of claim 7, wherein the frequency range bounder includes an output register coupled to the comparator, and wherein the comparator compares the control signal by comparing data values in the control signal with the upper and lower

values and latching the data values in between the upper and lower values into the output register.

9. The apparatus of claim 1, further comprising a drive circuit that receives the bounded control signal and that drives the oscillator in accordance with the bounded control signal.

10. The apparatus of claim 1, wherein the incoming video signal is a digital signal and the clock signal portion of the incoming video signal is program clock reference data for the digital signal.

A' cont'd

11. The apparatus of claim 1, wherein the incoming video signal is an analog signal and the clock signal portion of the incoming video signal is at least one of horizontal and vertical timing information embedded in the incoming video signal.

12. A frequency range bounder for limiting a frequency of an oscillator, comprising:

at least one threshold register that stores at least one threshold value; and

a receiver coupled to the threshold register that receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to a selected range.

13. The frequency range bounder of claim 12, wherein the receiver is an output multiplexer coupled to the threshold register, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range.

14. The apparatus of claim 12, wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value.

15. The apparatus of claim 14, wherein the receiver includes an output multiplexer that selects one of the upper value, the control signal, and the lower value as the bounded control signal and outputs the bounded control signal to the controlled oscillator to bound the oscillator frequency between an upper level and a lower level.

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16. The apparatus of claim 15, wherein the receiver further includes at least one of a high comparator and a low comparator coupled to the output multiplexer, wherein the high comparator compares the control signal with a high limit and the low comparator compares the control signal with a low limit, and wherein the output multiplexer outputs the upper value as the bounded control signal if the control signal is above the high limit and outputs the lower value as the bounded control signal if the control signal is below the low limit.

17. The frequency range bounder of claim 14, wherein the receiver includes at least one of a minimum function block coupled to the high limit register and a maximum function block coupled to the low limit register, wherein the minimum function block outputs the smaller of the control signal and the upper value and wherein the maximum function block outputs the larger of the control signal and the lower value as the bounded control signal.

18. The frequency range bounder of claim 14, wherein the receiver includes a comparator coupled to the high limit register and low limit register, wherein the comparator compares the control signal with the upper and lower values and outputs the

control signal to the output register if the control signal is between the upper and lower values.

19. The frequency range bounder of claim 18, further comprising an output register coupled to the comparator, and wherein the comparator compares the control signal by comparing data values in the control signal with the upper and lower values and latching the data values in between the upper and lower values into the output register.

20. A method for outputting an oscillator-generated clock signal for video reconstruction in a terminal, comprising the steps of:

receiving an incoming video signal in a control logic circuit with a phase locked loop;

phase locking to a clock signal portion of the incoming video signal; and

limiting the oscillator frequency to a selected range using a frequency range bounder in the phase locked loop, wherein the frequency range bounder receives a control signal and limits the oscillator frequency based on the control signal.

21. The method according to claim 20, further comprising the step of outputting a bounded control signal from the frequency range bounder to the oscillator to conduct the limiting step.

22. The method of claim 20, wherein the limiting step has the step of selecting one of an upper value, the control signal, and a lower value as the bounded control signal.

23. The method of claim 22, wherein the limiting step further has the steps of:

comparing the control signal with at least one of a high limit and a low limit;

outputting the upper value as the bounded control signal if the control signal is above the high limit; and

outputting the lower value as the bounded control signal if the control signal is below the low limit.

A' cancel.

24. The method of claim 20, wherein the incoming video signal is a digital signal and the clock signal portion of the incoming video signal is program clock reference data for the digital signal.

25. The method of claim 20, wherein the incoming video signal is an analog signal and the clock signal portion of the incoming video signal is at least one of horizontal and vertical timing information embedded in the incoming video signal.